UNIVERSITY OF NEBRASKA AT OMAHA
COURSE SYLLABUS/DESCRIPTION

Department and Course Number	CSCI 4350
Course Title	Computer Architecture
Course Coordinator	Azad Azadmanesh
Total Credits	3
Date of Last Revision	December 3, 2008

1.0 Course Description

1.1 Students are introduced to the technology and architecture of computers. The objectives are to introduce students to a large body of concepts and current trends in computer architecture, so that the design issues and their tradeoffs can be appreciated. Topics covered include top level view of computers, register level; cache memory and cache coherence; internal and external memory (disk, RAID, magnetic and optical); pipelined computer architecture; RISC versus CISC; and parallel processing.

1.2 For whom course is intended.
This is a core undergraduate computer science course.

1.1 Prerequisites of the course (Courses).
CSCI 3710 - Introduction to Digital Design and Computer Organization
CSCI 3320 - Data Structures

1.2 Prerequisites of the course (Topics).
- 1.2.1 Logic expressions
- 1.2.2 Design of Arithmetic units
- 1.2.3 Combinational and sequential logic design
- 1.2.4 Design of datapath with proper registers
- 1.2.5 Computer organization at the register transfer level
- 1.2.6 Internal memory design
- 1.2.7 Assembly language
- 1.2.8 Fundamental topics of Data Structures course.

1.3 Unusual circumstances of the course
None

2.0 Objectives

2.1 Students will learn a large body of concepts and current trends in computer architecture.
2.2 Students will learn about the design issues and their tradeoffs
2.3 Students will learn about performance parameters and related issues such as: speed up, utilization, throughput, bandwidth, response time, CPU & system times
2.4 Students will learn parallel processing, multiprocessor system design & tradeoffs

3.0 Content and Organization

Contact hours

3.1 Introduction 3.0
- 3.1.1 Computer Organization versus Computer Architecture
- 3.1.2 Computer Evolution and Performance
- 3.1.3 Pentium Evolution
- 3.1.4 Performance measures
  - 3.1.4.1 Response time
  - 3.1.4.2 Throughput
  - 3.1.4.3 Comparing design alternatives
  - 3.1.4.4 Benchmarking programs
  - 3.1.4.5 Average execution times
  - 3.1.4.6 Weighted execution times
  - 3.1.4.7 Speedup
  - 3.1.4.8 Clock cycles and instruction count
  - 3.1.4.9 MIPS

3.2 Top Level View of Computers 3.0
- 3.2.1 Computer components
- 3.2.2 Interconnection structures
- 3.2.3 Buses
  - 3.2.3.1 Synchronous versus Asynchronous communication
  - 3.2.3.2 Bus interconnections
  - 3.2.3.3 PCI bus system
  - 3.2.3.4 SCSI bus system

3.3 Cache Memory 8.0
- 3.3.1 Computer memory system overview
- 3.3.2 Cache memory principles
- 3.3.3 Elements of cache design
  - 3.3.3.1 Direct mapped
  - 3.3.3.2 Set associative
  - 3.3.3.3 Fully associative
  - 3.3.3.4 Miss, hits, and penalties
  - 3.3.3.5 Cache block replacement strategies
  - 3.3.3.6 Cache write strategies
  - 3.3.3.7 TLB, Pre-fetching
- 3.3.4 Alpha chip cache architecture
- 3.3.5 Cache coherence
  - 3.3.5.1 Centralized versus distributed memory
  - 3.3.5.2 Multilevel cache
  - 3.3.5.3 Directory based protocols
  - 3.3.5.4 Snoopy protocols

3.4 Internal Memory 6.0
- 3.4.1 Memory interleaving
- 3.4.2 Memory design out of smaller chips
- 3.4.3 Memory bandwidth
- 3.4.4 Virtual versus physical addresses

3.4.5 Page tables and address translation

3.5 External Memory
- 3.5.1 Introduction & performance relation to cache/memory/CPU — 3.0
- 3.5.2 Magnetic disk
- 3.5.3 RAID
- 3.5.4 Optical memory
- 3.5.5 Magnetic tape

3.6 Instruction Sets: — 2.0
- 3.6.1 MIPS instructions and addressing modes
- 3.6.2 MIPS instruction set architecture

3.7 Pipelined Processor Structure and Function — 2.0
- 3.7.1 Instruction cycle and pipelining
- 3.7.2 Pentium processor

3.8 RISC vs. CISC
- 3.8.1 Large register files
- 3.8.2 Compiler based register optimization
- 3.8.3 RISC and CISC architecture & controversy
- 3.8.4 Pipelining — 12.0
  - 3.8.4.1 Introduction
  - 3.8.4.2 MIPS pipeline cycles and micro-instructions
  - 3.8.4.3 MIPS stage and interstage architectures
  - 3.8.4.4 MIPS 4000
  - 3.8.4.5 Pipeline performance
  - 3.8.4.6 Hazards (data, control, structural)
  - 3.8.4.7 Data hazards
  - 3.8.4.8 Pipeline stalls
  - 3.8.4.9 Forwarding
  - 3.8.4.10 Instruction reordering
  - 3.8.4.11 Delay instructions
  - 3.8.4.12 Detection of stalls & forwarding

3.9 Parallel Processing
- 3.9.1 Taxonomy of parallel architectures — 3.0
- 3.9.2 Symmetric multiprocessors
- 3.9.3 Cache coherence and MESE protocol
- 3.9.4 Clusters